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ESD TILE GROWTH AND “SCALING”

In very simple terms, “scaling” is when electronic equipment manufacturers pack more capability into smaller packages.

Making “smart phones” smarter is a simple example of “scaling”. The phone stays the same size or gets smaller but it does more and more things.

To do “scaling”, the actual IC (integrated circuit) components need to be made smaller in order to fit into smaller spaces inside, for example, phones, GPS units or hand held medical devices.

However, IC components become more susceptible to Electro Static (ES) discharge damage the smaller that they get. (Ironically, the need for space also means that components historically used to protect against ES discharge are either reduced or eliminated from the device, despite the fact that the device is more susceptible to ES discharge damage)!

Today, during the manufacturing process, components are generally designed to withstand ES discharges of up to 2,000 volts but because of the need to make increasingly smaller and smarter electronics the goal over the next 5 years is to create manufacturing environments where components need only withstand 100 volts of ES discharge without any decline in manufacturing yields.

Therefore, the drive to “scale “ means that while manufacturers currently need only to create manufacturing environments that protect against ES discharges of 2,000 volts, over the next 5 years, these environments will need to protect against ES discharges of 100 volts or less.

This is a very ambitious goal but “scaling” is the next “frontier” and whoever wins the “scaling” war will win huge market share.

In turn, creating manufacturing environments that need to limit voltage discharge to 100 volts is a huge growth opportunity for VPI, as VPI tile can significantly contribute toward meeting this new manufacturing voltage discharge limit.

Specifically, in response to this increased risk of damage, ESD protection standards (such as ANSI 20.20 that encompasses everything from air conditioners to flooring) are being “elevated” by leading electronic manufacturing companies in response to the newly emerging 100 volt requirements.

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Here is a summary of evolving and “elevating” ESD standards as it relates to ESD flooring:

TILE ONLY TESTS

1. **NFPA 99** – Established in the 1970’s: tests tile at 500 volts. Worthless in today’s electronic manufacturing environment.
2. **ASTM F150** – Established in the 1980’s: tests tile at 100 volts. Fast becoming worthless in today’s electronic manufacturing environment.
3. **ANSI STM7.1; A RESISTANCE TEST**
Established in 2005: Tests tile at 10 volts. Fast becoming the standard test for ESD tile. VPI conforms to this standard at 10 volts within the conductive range. **PLEASE NOTE; STM7.1 CAN ONLY BE PASSED USING CONDUCTIVE TILE MEANING THE DEMAND FOR STATIC DISSIPATIVE TILES WILL DECLINE IN PROPORTION WITH THE INCREASE IN USE OF STM7.1**

Just testing the tile in a vacuum is limited so two additional flooring tests have been developed:

4. **ANSI STM97.1: A TILE AND PERSON RESISTANCE TEST.** This test is designed to determine total circuit resistivity by measuring the total path voltage must take through a person standing on an ESD floor. This is meant to simulate a stationary person working at a work station. This idea is not to be above 35 million ohms. VPI test results report that VPI Conductile tests below 1 million ohms.
5. **ANSI STM97.2: A TILE AND PERSON VOLTAGE TEST.** This test is designed to determine how much voltage a person can build up in their body walking across an ESD Floor. Below 100 volts is very good. To be at about 50 volts (or below) is excellent. VPI tests at about 50 volts.
6. **STM 97.2 is deemed to be a very important test as voltage discharge is a critical factor pertaining to” scaling”.** (Note: Shoe type does impact performance and VPI tests take this variable into account. Accordingly, VPI can recommend proper conductive footwear commonly available from industrial shoe suppliers. That, when used with VPI tile comply with STM97.2 as it relates to the 50 – 100 volt targets).

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